# DEVELOPMENT OF GRAPHENE AND SILICON NANOWIRES FOR <br> <br> PHOTOVOLTAIC AND FIELD ELECTRON <br> <br> PHOTOVOLTAIC AND FIELD ELECTRON <br> <br> EMISSION APPLICATIONS 

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By

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## Thesis Abstract

This thesis examines the development of low-dimensional carbon and silicon materials such as: Graphene (2-D) and Silicon Nanowire (1-D) using chemical vapor deposition techniques for photovoltaic and electron-field emission applications. Graphene is a two-dimensional crystal. It consists of a single layer of carbon atoms arranged in a honeycomb lattice, and its charge carriers are confined within a 2D plane. These charge carriers behave like mass-less Dirac particles and possess extremely high carrier mobilities. Silicon nanowire (SiNW), which is a quasi-one-dimensional structure, has attracted much research interest in the past decade due to its exceptional electrical and physical properties. The unique optical and electrical properties of graphene and SiNW make these materials useful for photovoltaic and electron-field emission applications.

The first system under investigation is graphene. In order to reach the ambitious goal of using graphene in photovoltaic and electron-field emission applications, one needs reliable methods for the large-scale production of high quality graphene films. Conventionally, graphene is prepared on transition metal catalyst surfaces and then transferred to substrates suitable for characterizations and applications. This transfer process adds the complexity of the processing and also reduces the intrinsic properties of graphene. Therefore, it becomes essential to develop direct growth techniques of graphene on insulting substrates including $\mathrm{SiO}_{2} / \mathrm{Si}$ wafers, glasses or plastic foils. Our research mainly focuses on the fabrication of high-quality, large-area graphene samples (Area $=1.5 \times 1.5 \mathrm{~cm}^{2}$ ) directly on $\mathrm{SiO}_{2} / \mathrm{Si}$ substrates primarily using chemical vapor deposition. The significant part of this research work is the synthesis of vertically oriented graphene by a vertical mass flow reactor through hotfilament chemical vapor deposition. The proposed growth mechanisms for both horizontally and vertically oriented graphene films are in good agreement with the spectroscopic characterizations. Additionally, other techniques such as micromechanical exfoliation of highly ordered pyrolytic graphite and chemical oxidation and reduction have been tried to synthesize bi-layer to few-layer graphene (FLG) samples on various substrates such as glass, Cu foil, ITO-coated glass, $\mathrm{SiO}_{2} / \mathrm{Si}$, $\mathrm{Cu} / \mathrm{SiO}_{2} /$ Si etc.

In order to study the behaviour of graphene in simple electronic devices, two basic solid state devices such as graphene-on-semiconductor junctions and electron-field emitter have been fabricated and studied both theoretically and experimentally. Graphene-on-silicon (p-type) device is fabricated and photovoltaic behaviour is studied while testing the device under dark and light conditions. Fieldemission from horizontally-oriented graphene sheets is a challenge due to less number of emission sites. Here, we have synthesized free-standing vertically-oriented FLG films directly on dielectric substrates by hot-filament chemical vapor deposition (HFCVD) without any catalyst or special substrate treatment. The fabricated FLGs are with a large smooth surface topography, oriented nearly vertical to the substrate and found to grow according to the Stranski-Krastanov growth mechanism. The feasibility of large area preparation and the low turn-on field of $22 \mathrm{~V} / \mu \mathrm{m}$ in addition to the large field enhancement factor of $\approx 6520$ and a field emission current density of $25 \mu \mathrm{~A} / \mathrm{cm}^{2}$ at an applied electric field of $44 \mathrm{~V} / \mu \mathrm{m}$ suggest that the vertically-oriented FLGs could be used as a potential edge emitter.

The second system under investigation is SiNW. A new technique for its growth is developed by a simple oxidation and reduction process of silicon wafers using a high temperature furnace. The plausible growth mechanism is also suggested. The process involves $\mathrm{H}_{2}$, in an inert atmosphere, reacts with thermally grown $\mathrm{SiO}_{2}$ on silicon at $1100^{\circ} \mathrm{C}$ enhancing the direct growth of nanowires on silicon wafers. High-resolution transmission electron microscopy studies show the crystalline silicon of diameter $\approx 30 \mathrm{~nm}$ as core with thin amorphous oxide shell of thickness as low as 2 nm . This structure of NW is confirmed by the selected area electron diffraction pattern. The grown SiNW posess a high aspect ratio of approximately 167; room temperature phonon confinement effect is also observed in the nanowires. This research of synthesizing crystalline SiNWs in a simple and economical way opens up vast opportunities for basic studies and nano-scale device applications.

